A 92k SPAD Time-Resolved Sensor in 0.13µm CIS Technology for PET/MRI Applications

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***Abstract*–This paper presents a 92k SPAD, 16×8 pixel sensor for PET imaging, implemented in 0.13µm low voltage CIS technology. Within each pixel, 720 SPADs are organized into high fill factor mini-SiPMs placed around a central logic block. The sensor demonstrates a new architecture for this application, providing a 100Msamples/s real time energy histogramming capability, as well as an on-chip discriminator for the recognition of gamma events and integration control for the automatic acquisition of event data. Preliminary gamma measurements demonstrate an energy resolution of 13.1% at 20ºC, improving to 11.3% at -20ºC.**

I. Introduction

The PhotoMultiplier Tube (PMT) is the long standing detector of choice in many nuclear imaging applications such as Positron Emission Tomography (PET). Such systems use a ring of detector modules, each containing a scintillator crystal and optical sensor, to detect pairs of Gamma photons resulting from radiotracer decays inside a patient. These detector modules must provide precise timing, energy, and positional information for each gamma photon detected to allow the point of emission to be precisely located.

In recent years, interest has grown in the realization of a low cost, compact, and magnetic field compatible replacement for the PMT. Solid-state solutions employing Single Photon Avalanche Diodes (SPADs) [1, 2] have been explored as a mass-manufacturable means of meeting these objectives. These detectors provide a discrete digital output pulse for every individual photon detected. An array of SPADs may be current-summed to produce an 'analogue' Silicon PhotoMultiplier (SiPM), providing a large photosensitive area at the expense of the ability to exploit the single photon detecting capability of the individual array elements [3]. Alternatively, fully digital SiPMs may be constructed by including processing logic on-chip. However, such sensors typically comprise a small number of large SPADs with only per-sensor or per-column photon time-stamping capability [2, 4].

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In this paper, we present a 92k SPAD, 16×8 pixel sensor implemented in 0.13µm low voltage CIS technology [5], with each pixel featuring four 180 SPAD *mini-SiPMs*, in-pixel counters, and Time to Digital Converters (TDCs) [6]. This new fully-digital SoC architecture for PET provides a 100Msamples/s real time energy histogramming capability and an on-chip discriminator for gamma event recognition.

II. High Fill Factor SiPM Approaches

Many SPAD-based sensors are composed of pixels containing a single SPAD surrounded by circuitry [7] (Fig. 1a). While such pixels can be well suited to particular applications, they provide a fill factor far too low for photon starved applications such as PET, in part due to the mandatory spacing introduced between each SPAD and the adjacent logic. As Fig. 2 demonstrates, the minimum achievable SPAD pitch is governed by one SPAD active region diameter, *d*, plus two cathode contact/guard ring thicknesses *g*, plus the width of the electronics.

Since PET does not require a fine spatial resolution, considerably larger pixels (with x and y dimensions of several hundred microns) are sufficient. A large number of SPADs can therefore be placed together to form a mini-SiPM, with one or more such blocks bordering a shared pixel logic area (Fig. 1b). Furthermore, the technique of well sharing [8] can be employed, whereby the SPADs are placed with overlapping cathode contacts. This decreases the SPAD pitch within the mini-SiPM regions to just $d + g$, as illustrated in Fig. 3. Using this technique, 720 (4×180) SPADs of 16.27µm active diameter are implemented in a compact 0.57×0.61mm^2 pixel area, along with the associated electronics, detailed in section III.

However, the use of well sharing requires the adoption of the positive drive bias configuration, whereby the full bias potential is applied directly to the deep NWELL SPAD cathode. Care must therefore be taken in low-voltage CMOS technologies to ensure that the high voltage placed on the NWELL does not cause parasitic junctions to break down, such as the vertical deep NWELL-substrate and lateral NWELL-PWELL junctions.

A number of approaches to this issue exist [9]. The lateral parasitic diode at the periphery of the mini-SiPM area is addressed here by the use of an undoped

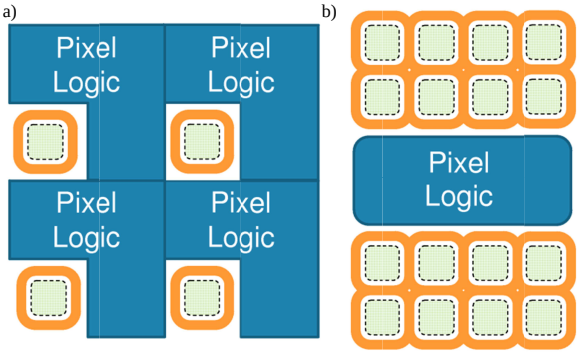

Fig. 1: a) Typical deep submicron CMOS SPAD sensor for applications such as 3D imaging or FLIM; b) sensor repartitioned as a SiPM for improved fill factor.

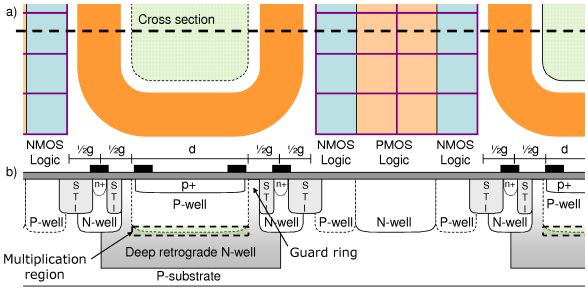

Fig. 2: a) Plan and b) cross-section views showing individual SPADs surrounded by logic in 130nm CMOS imaging technology.

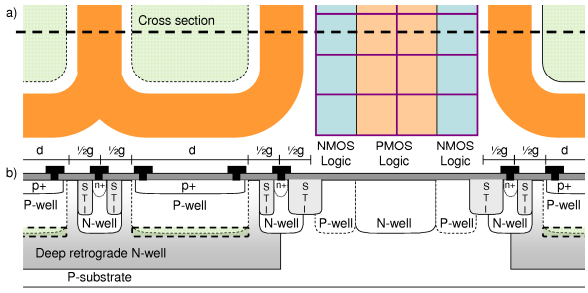

Fig. 3: a) Layout of shared SiPM with logic channel; b) cross-section showing device structure.

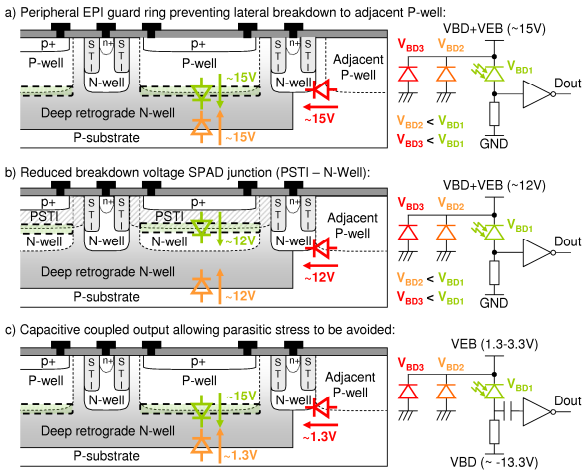

Fig. 4: Comparison of cathode well sharing strategies in a nanometer scale CMOS imaging process.

virtual guard ring around the SPAD region to prevent lateral breakdown (Fig. 4a).

Alternative solutions include the use of a lower-doped SPAD junction, which allows a lower bias voltage, or reconfiguration of the SPAD bias topology using a capacitive coupling (Fig. 4c).

III. Sensor Implementation

Fig. 5 illustrates the top level architecture of the sensor. To provide the required temporal, spatial, and energy information relating to each detected gamma photon, while suppressing the generation of such information for SPAD dark counts, the sensor has two main operating modes. While waiting for a gamma event in the idle mode, all photons detected by each pixel during a 10ns period (defined by an H-tree distributed clock) are counted. These pixel counts are hierarchically summed to produce a single, 16-bit total representing the instantaneous photon flux striking the sensor.

This real time histogram data is made available off chip via a 16-bit parallel output bus, while an on-chip discriminator module continually compares pairs of consecutive histogram codes to programmable threshold values. When these thresholds are exceeded, the system regards the light currently striking the sensor as a valid gamma scintillation event, and enters integration mode. The spatial distribution and total energy of the event are then captured by the pixels over a defined integration period. Even during integration, histogram data is made available off chip, thus providing a means for false event filtering and detection of multiple concurrent gamma events (scintillator pile-up).

The sensor also includes a number of ancillary blocks. A serial interface allows the configuration of sensor parameters such as integration time and discrimination thresholds. A programming system for the in-pixel SRAM cells allows the SPADs to be individually enabled or disabled, facilitating test and optimisation of SNR by disabling high-DCR SPADs. Finally, pixel data is read out by a row decoder following the completion of an event integration period. The pixel rows are sequentially requested to present their output data on shared column buses to be captured by a serialiser block. The 16-bit output bus is reconfigured to assign one pad per column, which is used to transmit the serialised pixel data off-chip.

Each pixel contains 4 independent 180 SPAD mini-SiPM arrays, each with associated electronics and a shared pixel logic block, as illustrated in Fig. 6. When instructed by the *accumulate* signal, distributed synchronously with the clock, the pixels accumulate the SPAD pulses counted in each clock cycle.

Each Mini-SiPM Interface and Counter (MIC) block (Fig. 7) contains a per-SPAD enable/disable SRAM cell, SPAD quenching circuitry, and an OR tree to combine the individual SPAD outputs into a single pulse train. Monostable devices are included after the first OR stage providing a pulse shortening function to prevent overlapping pulses from obscuring each other, termed temporal compression, as presented in [4]. This is critical for PET applications where the length of each

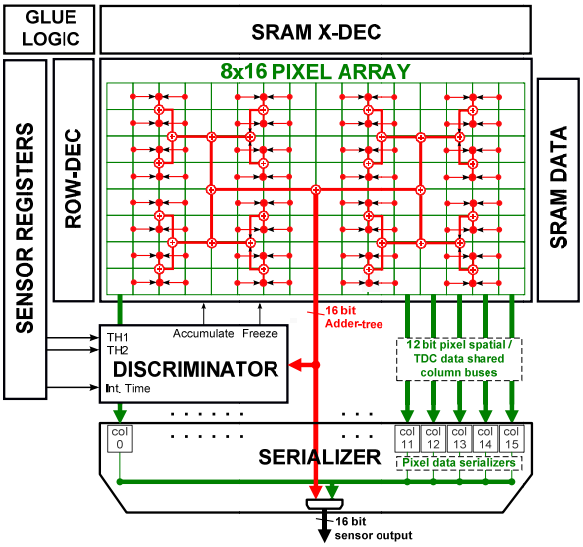

Fig. 5: Block diagram of the sensor architecture.

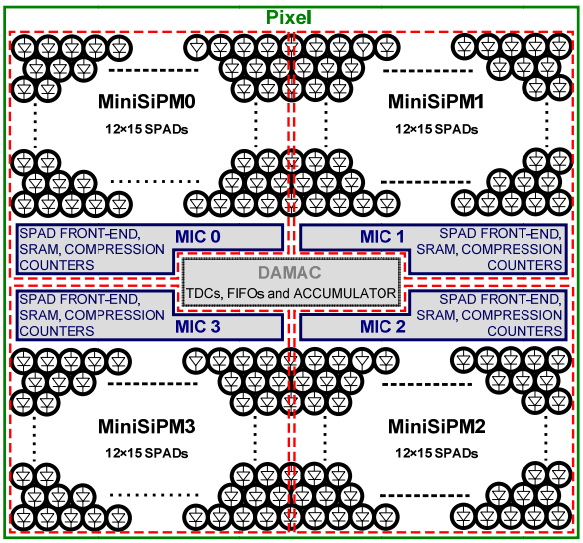

Fig. 6: Block diagram detailing the pixel architecture.

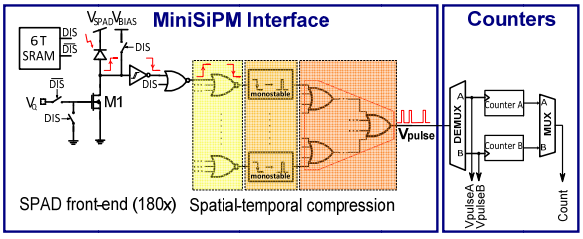

Fig. 7: Mini-SiPM Interface and Counter (MIC) blocks.

SPAD pulse (dead time) is typically comparable to the duration of the scintillation event. The positioning of the monostables after the first 3-input NOR stage introduces spatial compression, as only one of the 3 SPADs may contribute a pulse during a given event, which clearly represents a trade-off between pixel fill factor (limited by the total area occupied by monostables) and ability to avoid pile up.

A counter, also within the MIC block, sums the SPAD pulses generated during each clock cycle. This is implemented using a pair of ripple counters

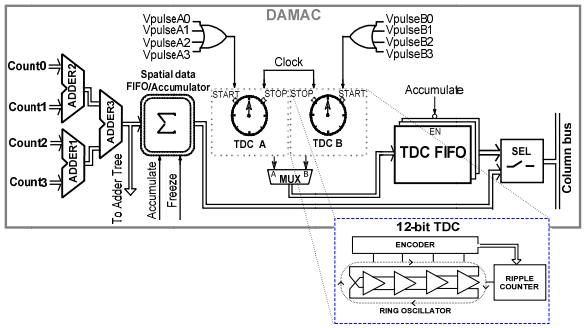

Fig. 8: Pixel DAta MAnaging Circuit (DAMAC).

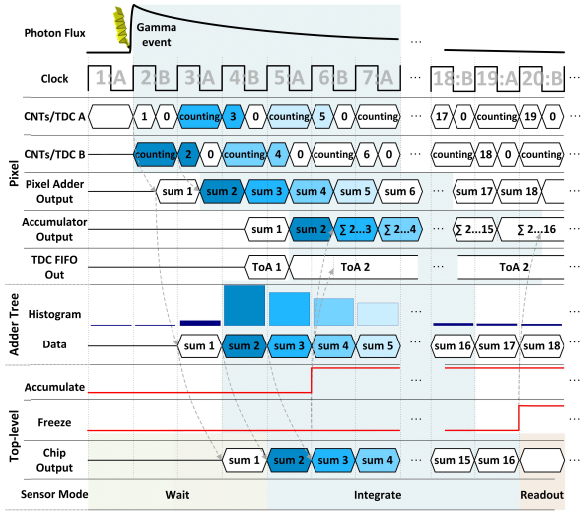

Fig. 9: System timing diagram. Integration begins with the CNT 2 bin, corresponding to the onset of the scintillator emission.

operating in a ping-pong fashion, so that one is integrating while the other is being read out and reset.

The pixel-level DAta MAnaging Circuit (DAMAC) then sums the four mini-SiPM counter outputs, as illustrated in Fig. 8. The summed values are passed to both the adder tree, which feeds the chip-level event discriminator and real-time histogram output, and an accumulator within the pixel. This integrates the counter data when instructed by the *accumulate* signal from the discriminator to calculate the total event energy detected by the pixel. Furthermore, a small 3-element FIFO implemented within the front end of the pixel accumulator accounts for the system's pipeline latency through the adder tree and discriminator. Consequently, integration begins with the bin values which caused the chip-level discriminator to trigger, and ends when the *freeze* signal is asserted after a programmable integration time. When read out, these individual pixel accumulator values provide an intensity 'image' showing the spatial distribution of scintillation light across the sensor, allowing the point of scintillation to be determined by off-chip processing. Similarly, the values may be summed to calculate the total energy of the incident gamma photon.

The DAMAC block also houses the in-pixel TDCs, which are arranged in a ping-pong pair. This allows one timestamp to be generated for every clock cycle with no intervening dead period. These TDC values are placed in their own FIFO which is frozen at the onset

of integration, preserving the timestamps of the crucial first few photons in the scintillation pulse, ready to be read out along with the spatial data. Fig. 9 illustrates the system timing, detailing the propagation of counter data through the system, resulting in a histogram mirroring the intensity of the incident scintillation light.

The discriminator's trigger output can be seen to transition in response to the SUM 2 and SUM 3 bins, with this decision being fed back to the pixel array resulting in the integration of bins SUM 2 onwards, and the preservation of the associated TOA 2 TDC code for later readout.

IV. Characterisation

The sensor, shown in Fig. 10, has been tested with a 3×3×5mm Teflon wrapped LYSO scintillator crystal irradiated by a 370kBq, 511keV Na22 gamma source. The system achieved an energy resolution of 13.1% FWHM at 20°C, and an improved 11.3% FWHM when cooled to -20°C.

A 70ps pulsed laser was used to measure the sensor's timing resolution, operated at low emitted power with a diffuser to reduce pile-up. Fig. 11 shows the histogram of TDC codes generated by a single pixel, exhibiting 263ps FWHM, compared to a reference system. When all valid TDC codes in a frame are averaged, the resulting FWHM is improved to 239ps, demonstrating that the per-pixel TDC architecture delivers improved timing performance with respect to per-column or per-sensor time-stamping. Table 1 provides a summary of key system performance metrics.

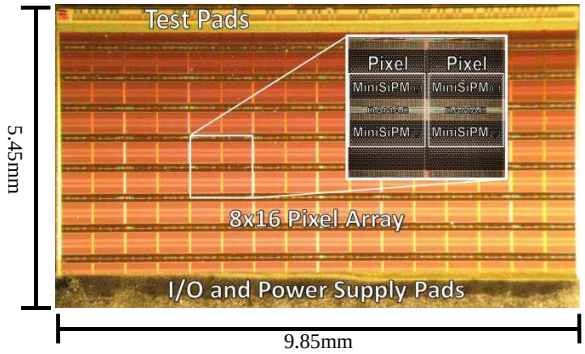

Fig. 10: Micrograph of sensor die with insert showing pixel detail.

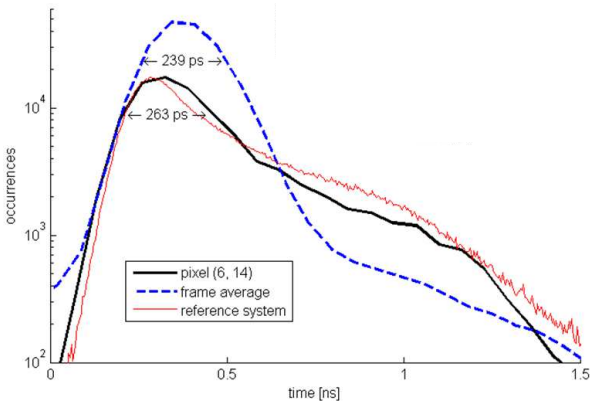

Fig. 11: System jitter characterized using pulsed laser illumination.

TABLE 1
PERFORMANCE SUMMARY

SPAD			
SPAD active diameter	16.27µm	SPAD pitch	19.27µm
Jitter @ 1.4V excess bias	150ps	Peak PDE @ 1.4V excess bias	28%
In-Pixel TDC			
TDC range (12-bit)	261.59ns	TDC resolution (1 LSB)	63.88ps
TDC INL	-3.8 to +2.3 LSB	TDC DNL	-0.24 to +0.28 LSB
TDC spatial uniformity (single chip)	0.75ps	TDC current consumption (single running TDC)	0.79mA
In-Pixel Counters			
Mini-SiPM counter depth	7-bit		
Pixel			
Pixel size	0.57×0.61mm^2	Pixel mini-SiPM dimensions	4×180-SPAD (15×12) mini-SiPMs
Sensor			
Process	1P4M 0.13µm CMOS imaging	Array size	8×16 pixels
Die size	9.85×5.425mm^2	Array fill factor	42.93%
Supply voltage	3.3V for IO 1.2V for core	Current consumption	40mA (dark) 100mA (light)
Readout interface			
Clock frequency	100MHz	Output data rate	1.6Gbps
Gamma detection performance for 370kBq 511keV Na22 source			
Energy resolution, 20ºC	13.1%	Energy resolution, -20ºC	11.3%

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